Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL MOUGEAT and MICHEL HARRAND

Appeal No. 1997-3842
Application No. 08/385,074

ON BRIEF

Before KRASS, RUGGIERO, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 12, 14 through 20, 22, 24 through 26, 28 through 30, and 35 through 44, which are all of the claims pending in this application.

Appellants' invention relates to an image predictor for digital image processing which includes a single search memory and plural read and write decoders which arrange the memory cells into independently readable blocks and independently writable blocks, respectively, such that each writable block

shares at least one memory cell with each readable block.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An image predictor for providing at least one target pixel in a preceding image, the preceding image being represented by a plurality of pixels, the at least one target pixel corresponding to a pixel in a current image shifted by a motion vector, the image predictor comprising:

a search memory comprising a plurality of memory cells each independently addressable in a read mode and a write mode;

a plurality of read decoders that arrange the memory cells into a corresponding plurality of simultaneously and independently readable blocks;

a write control circuit that writes data to the search memory that represents the plurality of pixels of the preceding image;

a plurality of write decoders that arrange the memory cells into a plurality of independently writable blocks, each of the plurality of independently writable blocks sharing at least one memory cell with each of the plurality of simultaneously and independently readable blocks, the plurality of write decoders arranging the memory cells so that when the data representing the plurality of pixels of the preceding image is written to the search memory, each one of said plurality of pixels is stored within a separate readable block from its adjacent pixels; and

a read control circuit that reads data from at least one memory cell, selected in response to the motion vector, that represents the at least one target pixel.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Hirano et al. (Hirano)	4,460,923	Jul. 17, 1984
Langlais et al. (Langlais)	5,181,229	Jan. 19, 1993
		(filed Dec. 28, 1989)

Claims 1 through 10, 14 through 20, 22, 24 through 26, 28 through 30, and 35 through 44 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hirano.

Claims 11 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hirano in view of Langlais.

Reference is made to the Examiner's Answer (Paper No. 33, mailed January 7, 1997) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 32, filed July 3, 1996) and Reply Brief (Paper No. 34, filed March 10, 1997) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejections of claims 1

through 12, 14 through 20, 22, 24 through 26, 28 through 30, and 35 through 44.

Each of independent claims 1, 16, 25, 36, 37, and 38 recites, in pertinent part, plural read decoders and write decoders[1], with the decoders arranging the memory cells of a search memory into simultaneously and independently readable blocks and independently writable blocks, respectively. Each claim further requires that each writable block shares at least one memory cell with each readable block.

The examiner states (Answer, page 13) that "each one of the picture element datas, i.e. X1, X2 ... X16, A1, ... A8 is considered a block of data." He continues (Answer, page 14) that "each one of the blocks of data as shown in Figure 8-11a of Hirano contains a memory cell that is writable and readable, and as such, the particular limitation of 'each of the writable blocks shares at least one memory cell with each of the readable blocks' as argued by the appellants is nevertheless being considered met by Hirano." We cannot agree

[1] Claim 16 recites a means for arranging the cells rather than specifying decoders.

with the examiner's conclusion, even assuming that his initial assumptions are correct. In Figure 8-11a, each writable block (according to the examiner's definition) has data in common with one readable block (again according to the examiner's definition). However, the claim requires that each writable block share a memory cell with each readable block, not just one. Thus, contrary to the examiner's assertion, Hirano fails to meet the claim limitation.

Further, as stated above, each independent claim requires that each block of memory cells be simultaneously and independently readable. The examiner explains (Answer, page 13) that x1 to x4 are simultaneously output by arithmetic units 8-1 to 8-4, respectively, and concludes (Answer, page 14) that the memory cells, therefore, are simultaneously readable. The examiner's position becomes a bit clearer at page 15 of the Answer, where the examiner clarifies that "since Hirano shows an example wherein arithmetic units 8-1 to 8-4 outputs x1 to x4, respectively ..., from memory 8-11a, it is considered obvious if not inherent that memory 8-11a is being accessed by all of the arithmetic units 8-1 to 8-4." In other words, the examiner apparently believes that all four

arithmetic units read from the same memory 8-11a, and that they do so simultaneously to output x1 to x4. Thus, as advanced by the examiner, since each entry of 8-11a is defined as a block, and four blocks must be addressed to output the four picture elements, the blocks are simultaneously readable.

However, as argued by appellants (Brief, page 10), memory 8-11a does not include multiple blocks that can be read simultaneously. Hirano (column 10, lines 20-21) refers to "the two-dimensional memories in the arithmetic units 8-2 through 8-4." Thus, each arithmetic unit includes its own memory 8-11a, and each outputs a different element. Consequently, that x1 through x4 are output simultaneously is irrelevant to the question of simultaneous addressability of the blocks of a single memory. We find no evidence that the blocks (as defined by the examiner) in any one of the memories are simultaneously addressable, and, in fact, the output of a single picture element by each arithmetic unit suggests that they the blocks are individually addressable, not simultaneously addressable, as required by the claims.

As to the read and write decoders, both the examiner (Answer, page 7) and appellants (Brief, page 10) agree that

there must be one read decoder and one write decoder for reading and writing a picture element from and to memory 8-11a, respectively.

However, the examiner asserts (Answer, page 13) that "multiple read and write decoders are ... used when the memory 8-11a is being accessed/written in a parallel fashion by arithmetic units 8-1, 8-2, 8-3, and 8-4 so as to provide the picture elements x1, x2, x3, and x4, respectively for example, within memory 8-11a." Such a conclusion, however, is based on the presumption that all four arithmetic units use the same memory, which we have determined above to be inaccurate. Thus, the examiner has no basis for his assertion that plural decoders are used for memory 8-11a. Further, appellant points out (Brief, page 10) that Hirano does not include plural decoders, because plural decoders are unnecessary in Hirano's system, since only a single element is read or written at a time in each of the memories. Accordingly, Hirano fails to meet the limitation of plural read and write decoders found in each of the independent claims.

Since Hirano fails to meet several of the limitations recited in each independent claim, the examiner has failed to

establish a prima facie case of obviousness. Therefore, we cannot sustain the rejection of claims 1, 16, 25, and 36 through 38, nor their dependents, claims 2 through 10, 14, 15, 17 through 20, 22, 24, 26, 28 through 30, 35, and 39 through 44.

Regarding the rejection of claims 11 and 12 over Hirano in view of Langlais, claims 11 and 12 ultimately depend from claim 1 and therefore include all of the limitations of claim 1 found lacking from Hirano. Langlais fails to cure the deficiencies of Hirano noted above. Accordingly, we cannot sustain the rejection of claims 11 and 12.

As a side note, throughout the Answer, the examiner states his opinion as to Hirano's disclosure. However, what the examiner believes is not the standard for obviousness. In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a **factual** basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is required to make the **factual** determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ

459, 467 (1966). Accordingly, only the evidence and factual determinations presented by the examiner were considered in rendering this decision, and not the examiner's opinions.

CONCLUSION

The decision of the examiner rejecting claims 1 through 12, 14 through 20, 22, 24 through 26, 28 through 30, and 35 through 44 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
JOSEPH F. RUGGIERO Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

apg/vsh

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